



# **Intel® Thunderbolt™ Release Notes For Ice-Lake Integrated Thunderbolt (iTBT) B-Step**

**Release Notes - NDA**

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***February 2019***

***Revision 35.0***

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## ***Audience***

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This document intended for use by OEM software developers, test and validation engineers, and system integrators.



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## Revision History

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Revision Number	Description	Revision Date
26.0	Initial release for iTBT B-Step	May 2018
27.0	ICL Pre-Alpha iTBT B-step release	August 2018
28.0	ICL-Y Pre-Alpha iTBT B-step release	August 2018
29.0	ICL-U/Y iTBT B-step release	October 2018
30.0	ICL-U/Y iTBT B-step release	October 2018
31.0	ICL-U/Y iTBT B-step release	October 2018
32.0	ICL-U/Y iTBT B-step release	November 2018
33.0	ICL-U/Y iTBT B-step release	January 2019
34.0	ICL-U/Y iTBT B-step release	January 2019
35.0	ICL-U/Y iTBT B-step release	February 2019



# 1 Introduction

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## 1.1 Scope of Document

This document provides component-level details of the downloaded release and the contents of each folder in the release.

## 1.2 Acronyms

Term	Description
TBT	Thunderbolt
HR	Host Router
EP	End-Point
AIC	Add-In Card
LR	Light Ridge (Thunderbolt)
PR	Port Ridge (Thunderbolt)
CR	Cactus Ridge (Thunderbolt)
RR	Redwood Ridge (Thunderbolt)
FR	Falcon Ridge (Thunderbolt 2)
AR	Alpine Ridge (Thunderbolt 3)
TR	Titan Ridge (Thunderbolt 3)
YFL	Yosemite Falls
ICL	Ice Lake
DP	Display Port
CM	Connection Manager
LC	Link Controller
HDCP	High-bandwidth Digital Content Protection
DB	Delta Bridge – TBT Retimer
P2P	Peer-to-Peer

## 1.3 Naming Convention

<project name>\_<Si stepping>\_<image rev>.bin

For example,  
 <project name>:  
 YFL, AR, TR, etc.

YFL\_A0\_Rev10.bin – Yosemite Falls A0 stepping Revision 10



## 2 Features Supported

Supported = ✓ Limited Support = ⚠ Not Supported = ✘

Technology	Support
Thunderbolt Link 20/40G (Rounded)	✓
Thunderbolt Link 20.3/40.6G (Non-Rounded)	✓
DP Tunnel	✓
PCIe traffic	✓
RTD3 – require full platform BKC support	✓
TBT Wake	✓
Sx	✓
Thunderbolt Link Power Management (CLx)	✓
P2P	✓



### 3 *New Features—RCRs*

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<b>RCR #</b>	<b>Title</b>	<b>Change Info</b>	<b>Status</b>
	<b>TBT RTD3 Support</b>	Added TBT RTD3 support.	Implemented in Rev <b>33.0</b>
	<b>TXFFE scan</b>	Added optional config (backward compatible) to ignore Retimer default TXFFE preset.	Implemented in Rev <b>33.0</b>



## 4 Issue Status Definitions

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This document provides sightings and bugs report for Integrated Thunderbolt SKUs. At the time of a milestone release, this report will be distributed with the Intel® TBT Release and will provide information on new issues and the status of old issues (replacing the Release Notes document).

**Closed Issues:** This category will only display closed issues within the current Intel® TBT release. After each release, old issues will be dropped down to the "Archive" section and then new closed issues will take its place back up top for the next release. If an issue is posted in this section, it will indicate that the issue has been verified and fixed within the one that is being released.

**Known Issues:** This category will display all Known Issues since the initial release and will remain in this section until fixed or noted otherwise. "Known Issues" are still under investigation and may or may not be root caused.

**Archive – Fixes in Previous releases:** This category will display all closed issues that were closed in their respected release#. This section will serve as a history of fixed issues.

**Sightings listed in this document apply to the Integrated Thunderbolt SKUs unless noted otherwise in this document or in the sightings tracking systems.**



## 4.1 Fixed Issues in this Release

Issue Closed in Release #	Title	Details	Affected SKUs
35.0	<b>CATERR during D3 to D0 transition</b>	<b>Sighting #:</b> <a href="#">1306170663</a> <b>Affected Component:</b> LC <b>Fix:</b> WA for CATERR that is caused due to TBT DMA transition from D3 to D0	<b>All</b>
35.0	<b>No P2P after unload driver (2 inter domain connected notifications)</b>	<b>Sighting #:</b> <a href="#">1306064331</a> <b>Affected Component:</b> CM <b>Impact:</b> We get "2 inter-domain connected" notifications <b>Fix:</b> The memory override is fixed which caused the "2 inter-domain connected" notifications	<b>All</b>



## 4.2 Known Issues—To Date

Issue Found in Release #	Title	Details	Affected SKUs
33.0	<b>CATERR on Restart entry in RTD3 supported systems</b>	<b>Sighting #:</b> 1306152223 <b>Affected Component:</b> CM <b>Impact:</b> CATERR is seen during restart entry when RTD3 is enabled.	<b>All</b>
29.0	<b>CATERR on Sx entry in RTD3 supported systems</b>	<b>Sighting #:</b> 1305909590, 1605359999 <b>Affected Component:</b> PM <b>Impact:</b> System throws CATERR on Sx entry when RTD3 is enabled.	<b>All</b>



### 4.3 Archive—Fixes in Previous Releases

Issue Fixed in Release #	Title	Details	Affected SKUs
34.0	<b>DP plug state close to C10 entry</b>	<b>Sighting #:</b> 1306064679 <b>Affected Component:</b> CP <b>Fix:</b> Fix for a corner case where LC might change the DP plug state, where monitor goes to sleep, close to C10 entry.	<b>All</b>
33.0	<b>Redundant DP plug events</b>	<b>Sighting #:</b> 1408276904 <b>Affected Component:</b> CP <b>Impact:</b> DP adapter ports on the thunderbolt controller, were sending plug event packets even when no device was connected. The fix is to block redundant DP plug events after C10.	<b>All</b>
33.0	<b>P2P connection</b>	<b>Sighting #:</b> 1305999339 <b>Affected Component:</b> CM <b>Impact:</b> P2P functionality is not working when P2P connection is done during/after Sx cycle. This is addressed by handling CM-Driver interaction.	<b>All</b>
33.0	<b>CATERR on Sx Entry</b>	<b>Sighting #:</b> 1305909590 <b>Affected Component:</b> LC <b>Impact:</b> System throws CATERR on Sx Entry with TBT Legacy Devices (Port Ridge). This is addressed by Sx transition LC handling.	<b>All</b>
32.0	<b>System hung running S4 on SNDW</b>	<b>Sighting #:</b> 1407945522 <b>Affected Component:</b> LC <b>Impact:</b> System had a soft hang error when running S4 cycles on SNDW. The MCA error showed that the PMC was hung waiting for ACK to comeback for <i>ForcePowerGate POK</i> signal.	<b>All</b>
32.0	<b>CATERR on S5 cycles</b>	<b>Sighting #:</b> 1606028956 <b>Affected Component:</b> LC <b>Impact:</b> SUT was hung with CATERR on doing S3 after warm rest cycle without any TBT device attached.	<b>All</b>
31.0	<b>No FW CM mode</b>	<b>Sighting #:</b> N/A <b>Affected Component:</b> CP <b>Impact:</b> Bug fix entrance flag to OS CM functionality	<b>All</b>



Issue Fixed in Release #	Title	Details	Affected SKUs
31.0	<b>PM_PME wake signal policy in OS CM configurations</b>	<b>Sighting # :</b> <a href="#">1306026133</a> <b>Affected Component:</b> CP <b>Impact:</b> To prevent auto wake of the ICL system in Sx, assert PM_PME wake signal only if DMA is in D3 and not SX entry.	<b>All</b>
30.0	<b>System auto wake on S3 and S4</b>	<b>Sighting # :</b> 1606710127 <b>Affected Component:</b> LC <b>Impact:</b> Fix for system auto wake on S3 and S4 entry with USB/DP devices connected on USB Type-C port	<b>All</b>
29.0	<b>AUX training time</b>	<b>Sighting #:</b> N/A <b>Affected Component:</b> DP <b>Impact:</b> Reduce number of defers by extending the AUX timeout to 400us	<b>All</b>
29.0	<b>Tile display</b>	<b>Sighting #:</b> <a href="#">1505666326</a> <b>Affected Component:</b> DP <b>Impact:</b> TBT3 Display blanks out while hot plug to TBT Ports in S0 State. Issue fixed through DP path reset on re-training to prevent training issues on certain tile displays	<b>All</b>
29.0	<b>Auto wake from RTD3</b>	<b>Sighting #:</b> N/A <b>Affected Component:</b> DMA <b>Impact:</b> Disable PM_PME transmission during IMR load, which is initiated as a result of reset given to iTBT on RTD3 entry.	<b>All</b>
29.0	<b>P2P disconnect failure</b>	<b>Sighting #:</b> <a href="#">1605340575</a> <b>Affected Component:</b> CM <b>Impact:</b> P2P path teardown was not happening after unplug between ICL to ICL and ICL to discrete TBT controller.	<b>All</b>
28.0	<b>System auto wake from Sx with DP monitor connected behind TR device</b>	<b>Sighting #:</b> <a href="#">1605458800</a> <b>Affected Component:</b> LC <b>Impact:</b> Disable Assert PME if DMA enter D3_HOT and DP is active or USB not in U3 state.	<b>All</b>
27.0	<b>DisplayPort tunneling failure with AR device</b>	<b>Sighting #:</b> <a href="#">1505738029</a> <b>Affected Component:</b> DP <b>Impact:</b> DP/HDMI display is not working behind TBT3 AR Docks, which is fixed by clock synchronization (TMU) adjustment when tunneled with legacy ridge.	<b>All</b>
26.0	<b>Thunderbolt enumeration on S3 exit</b>	<b>Sighting #:</b> <a href="#">1806108862</a> <b>Affected Component:</b> PM <b>Impact:</b> TBT enumeration fails after S3 exit waiting for LSx communication.	<b>All</b>
26.0	<b>Monitor off after plug-unplug</b>	<b>Sighting #:</b> <a href="#">1806128661</a> <b>Affected Component:</b> DP <b>Impact:</b> Monitor is off after CIO link is down and up again.	<b>All</b>



Issue Fixed in Release #	Title	Details	Affected SKUs
25.0	<b>System hang on Sx/warm reset</b>	<b>Sighting #:</b> <a href="#">1305644456</a> <b>Affected Component:</b> PM <b>Impact:</b> Sx and warm reset with TBT device connected cause system hang. <b>Workaround:</b> Disconnect TBT device and perform reset/Sx	<b>All</b>
25.0	<b>Minimum of PKC3 on TBT</b>	<b>Sighting #:</b> <a href="#">1305638487</a> <b>Affected Component:</b> System Power <b>Impact:</b> After connecting TBT device, processor package C-state gets demoted from PKC8 to PKC3.	<b>All</b>
25.0	<b>LSx Flows</b>	<b>Sighting #:</b> <b>Affected Component:</b> LC <b>Impact:</b> Asserting LSTX low during no wake Sx, fixes LSx handling on Sx.	<b>All</b>
25.0	<b>CATERR on Sx</b>	<b>Sighting #:</b> <a href="#">1806108862</a> <b>Affected Component:</b> PM <b>Impact:</b> Sx and warm reset with TBT device connected cause CATERR. <b>Workaround:</b> Disconnect TBT device and perform reset/Sx.	<b>All</b>