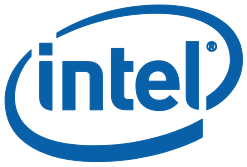

Thunderbolt™ Release Notes For Ice-Lake Integrated Thunderbolt (iTBT) D-Step

Release Notes - NDA

February 2020

Revision 80.0

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This document contains information on products in the design phase of development.

Audience

This document intended for use by OEM software developers, test and validation engineers, and system integrators.

Contents

Revision History

Revision Number	Description	Revision Date
60.0	Initial release for iTBT D-Step	November 8, 2018
61.0	ICL-U/Y iTBT D-step release	January 20, 2019
62.0	ICL-U/Y iTBT D-step release	February 4, 2019
63.0	ICL-U/Y iTBT D-step release	March 7,2019
64.0	ICL-U/Y iTBT D-step release	March 18,2019
66.0	ICL-U/Y iTBT D-step release	April 3,2019
67.0	ICL-U/Y iTBT D-step release	April 11,2019
68.0	ICL-U/Y iTBT D-step release	April 18,2019
69.0	ICL-U/Y iTBT D-step release	April 24,2019
70.0	ICL-U/Y iTBT D-step release	May 1,2019
71.0	ICL-U/Y iTBT D-step release	May 23,2019
72.0	ICL-U/Y iTBT D-step release	June 12,2019
73.0	ICL-U/Y iTBT D-step release	July 12,2019
74.0	ICL-U/Y iTBT D-step release	August 1,2019
75.0	ICL-U/Y iTBT D-step release	September 5,2019
76.0	ICL-U/Y iTBT D-step release	October 10 ,2019
77.0	ICL-U/Y iTBT D-step release	November 19, 2019
79.0	ICL-U/Y iTBT D-step release	January 9,2020
80.0	ICL-U/Y iTBT D-step release	February 13, 2020

1 Introduction

1.1 Scope of Document

This document provides component-level details of the downloaded release and the contents of each folder in the release.

1.2 Acronyms

Term	Description
TBT	Thunderbolt™
HR	Host Router
EP	End-Point
AIC	Add-In Card
LR	Light Ridge (Thunderbolt™)
PR	Port Ridge (Thunderbolt™)
CR	Cactus Ridge (Thunderbolt™)
RR	Redwood Ridge (Thunderbolt™)
FR	Falcon Ridge (Thunderbolt™ 2)
AR	Alpine Ridge (Thunderbolt™ 3)
TR	Titan Ridge (Thunderbolt™ 3)
YFL	Yosemite Falls
ICL	Ice Lake
DP	Display Port
CM	Connection Manager
LC	Link Controller
HDCP	High-bandwidth Digital Content Protection
DB	Delta Bridge – TBT Retimer
P2P	Peer-to-Peer

1.3 Naming Convention

<project name>_<Si stepping>_<image rev>.bin

For example,
<project name>:
YFL, AR, TR, etc.

YFL_D0_Rev1.bin – Yosemite Falls D0 stepping Revision 1

2 Features Supported

Supported = ✓ Limited Support = ⚠ Not Supported = ✘

Technology	Support
Thunderbolt Link 20/40G (Rounded)	✓
Thunderbolt Link 20.3/40.6G (Non-Rounded)	✓
DP Tunnel	✓
PCIe traffic	✓
RTD3	✓
TBT Wake	✓
Sx	✓
Thunderbolt Link Power Management (CLx)	⚠
P2P	✓

3 New Features—RCRs

RCR #	Title	Change Info	Status
80.0	New CM memory-based logger	**Sighting #:** 1306843592 **Affected Component:** CM **Fix:** Added CM FW memory-based logger capability (works together with NPK).	All
72.0	Speed setting for testing purpose	**Sighting #:** 1807771943 **Affected Component:** LC **Fix:** Added support for *Force Ports Speed* command.	All

4 Issue Status Definitions

This document provides sightings and bugs report for Integrated Thunderbolt™ SKUs. At the time of a milestone release, this report will be distributed with the Intel® TBT Release and will provide information on new issues and the status of old issues (replacing the Release Notes document).

Closed Issues: This category will only display closed issues within the current Intel® TBT release. After each release, old issues will be dropped down to the "Archive" section and then new closed issues will take its place back up top for the next release. If an issue is posted in this section, it will indicate that the issue has been verified and fixed within the one that is being released.

Known Issues: This category will display all Known Issues since the initial release and will remain in this section until fixed or noted otherwise. "Known Issues" are still under investigation and may or may not be root caused.

Archive – Fixes in Previous releases: This category will display all closed issues that were closed in their respected release#. This section will serve as a history of fixed issues.

Sightings listed in this document apply to the Integrated Thunderbolt™ SKUs unless noted otherwise in this document or in the sightings tracking systems.

4.1 Fixed Issues in this Release

Issue Closed in Release #	Title	Details	Affected SKUs
80.0	**Some monitor flash after the display is up when both MST is on and DM is running**	**Sighting #:** 2209552982 **Affected Component:** DP **Impact:** Some corner cases (timing) can cause mismatched aux request / response, which can cause link training failure. Which results in monitor to flash after normal display when Multi-Stream Transport is on and Display Manager (DM) is running. **Fix:** Fixed the interface between firmware and hardware accelerator.	**All**
80.0	**DP adapter resets every 5 sec with LTTPR enabled in DP Tunnel**	**Sighting #:** 1307052557 **Affected Component:** DP **Impact:** DP_IN does not set the CMN_CAP valid bit to CM and as a result no video. **Fix:** Fix in capabilities flow in LTTPR non-transparent mode.	**All**
80.0	**Specific Type-C monitor connected to TBT port on specific dock fails to display**	**Sighting #:** 1307006871 **Affected Component:** CM **Impact:** Connect Type-C monitor to TBT port on specific dock fails to display. **Fix:** Removed the unneeded Firmware (FW) writes which were introduced in previous work around for MST display.	**All**

4.2 Known Issues—To Date

Issue Found in Release #	Title	Details	Affected SKUs

4.3 Archive—Fixes in Previous Releases

Issue Fixed in Release #	Title	Details	Affected SKUs
79.0	**Flicker on wake from sleep with 6k display**	**Sighting #:** 2209620783 **Affected Component:** DP and CM **Impact:** Flicker is observed on wake from sleep with the 6K display. **Fix:** After TBT is locked in equalization state, TBT will replay as not locked for the first status read, for the second read after 16ms it will replay with lock. CM set TMU_STABLE CONFIGURATION in TMU port space, that set the minimum cycle for TMU clock stable to 8 (instead of infinite).	**All**
79.0	**Display Power (600h) states transitions are not forwarded downstream to the TBT node to sinks during sleep wake transitions**	**Sighting #:** 1307169330 **Affected Component:** DP **Impact:** Display Power (600h) states transitions are not forwarded downstream to the TBT node to sinks during sleep wake transitions. **Fix:** Register read of dpcd 0x600 is now sending to the monitor during wake transitions.	**All**
79.0	**Icelake single lane self-powered devices will not train**	**Sighting #:** 1307096441 **Affected Component:** LC **Impact:** When the self-powered Port Ridge device is plugged in to Legacy adapter, which is plugged into the system, Link's does not show up. **Fix:** LC should ignore the first LSM request, if single lane self-powered legacy device is connected.	**All**
79.0	**ICL Boot Camp: TBT display does not light up at boot intermittently**	**Sighting #:** 1306821292 **Affected Component:** CP **Impact:** TBT display does not light up at boot intermittently. **Fix:** Fix for missing plug packet on DPIN port # 5 after S3. i.e. CM FW should query dp_in resources and if marked as 'can be used by CM', store it as available dp_in.	**All**
79.0	**Unplugging while going into S0ix sleep leads to no links on wake with legacy adapters**	**Sighting #:** 14010547529 **Affected Component:** LC **Impact:** Unplugging while going into S0ix sleep leads to no links on wake with legacy adapters. **Fix:** LC drive LSTX to low after sending LRoff during Sx/S0ix entry flow with unconfigured device and "wake on CIO connect" is set.	**All**

Issue Fixed in Release #	Title	Details	Affected SKUs
79.0	**System does not dark wake when a Thunderbolt 2 device is hot plugged**	**Sighting #:** 1307105150 **Affected Component:** LC **Impact:** System does not wake when a Thunderbolt 2 device is hot plugged. **Fix:** Config wake in LSx if empty TBT2->TBT3 adapter is connected.	**All**
77.0	**Error upon resume from S3 and continue with video playback**	**Sighting #:** 1306976485 **Affected Component:** CM. **Impact:** When the system wakes up from the S3 state and continues with the video playback error is noticed. **Fix:** CM clean up on boot camp in apple mode checking for SX flows.	**All**
76.0	**S0ix wakes while TBT Interdomain is connected**	**Sighting #:** 2209195015 **Affected Component:** LC **Impact:** ICL Interdomain (Cross domain) S0ix wakes on sleep. **Fix:** LC doesn't config wake in LSx during S0ix entry if wake events are cleared.	**All**
76.0	**No DP Tunneling after switching from SW CM to FW CM**	**Sighting #:** 1306821292 **Affected Component:** CM **Impact:** When switching from SW CM to FW CM, no DP tunnel due to misalignment in DP resources. **Fix:** FM CM will clean up the topology configuration made by SW CM before switching to operational mode.	**All**
75.0	**System cannot enter PKG C3 during P2P connection**	**Sighting #:** 1306697139 **Affected Component:** CM **Impact:** System cannot enter Package C state during P2P connection. **Fix:** Increase the number of IM connected request retries from 2 to 10 as defined by Apple's IM doc.	**All**
74.0	**Spurious HPD interrupt with TBT2 monitor after warm reset**	**Sighting #:** 1409349284 **Affected Component:** DP **Impact:** Spurious HPD interrupt with Thunderbolt2 monitor after warm reset. **Fix:** Detection of Interrupt (IRQ) from HW and generate the Interrupt (IRQ) from dp_in to upstream and in case of using TBT 2 monitor, Filter on HPD/IRQ detection.	**All**

Issue Fixed in Release #	Title	Details	Affected SKUs
73.0	**Displays connected to TBT3 dock blank out while transferring data from TBT3 Storage to SUT**	**Sighting #:** 1807870871 **Affected Component:** CM **Impact:** Displays connected to the TBT3 dock blanks out while transferring data from TBT3 Storage to SUT which is connected behind the TBT3 dock. **Fix:** Workaround for this issue is changing back-pressure threshold due to overrun in CIO Switch.	**All**
73.0	**No inter domain connection notification upon boot from S5 with signed AIC**	**Sighting #:** 1306569411 **Affected Component:** CM **Impact:** No inter domain connection notification is sent upon booting from S5 state with signed add in card. **Fix:** Handling IM not up after S5 state with signed host.	**All**
73.0	**Takes ~20 seconds to configuring GR PCIE tunnel if TR is connected in the middle**	**Sighting #:** 1306506880 **Affected Component:** CM **Impact:** It takes ~20 seconds to configuring GR PCIE tunnel if TR is connected in the middle **Fix:** Fix PCIE path configuration timing from 20 seconds to 2 seconds.	**All**
73.0	**LSM error counter is up after un-plug**	**Sighting #:** 1306183725 **Affected Component:** CP **Impact:** LSM error counter is up after un-plug. **Fix:** Link FSM polling adjustments are made to fix this issue.	**All**
73.0	**CM not configuring LR device even in Boot Camp**	**Sighting #:** 1306569746 **Affected Component:** CM **Impact:** CM not configuring LR device even in Boot Camp (i.e. TBT1 devices are not enumerating in boot camp) **Fix:** Fix for LR (TBT 1) device connectivity in boot camp.	**All**
72.0	**Hotplug TBT3 TR dock with Display connected blanks out and flickering on eDP**	**Sighting #:** 1607272295 **Affected Component:** DP **Impact:** Display blanks out on external monitor when connected behind TBT3 TR docks with 2 Displays and flickering on eDP when hot plugged in S0 state or during cold boot with Non Transparent LTTPR Driver **Fix:** Fix DPRX_READ handshake with CM by reducing dependency of AUX order in LTTPR.	**All**
71.0	**TBT-SSD not enumerating in BIOS and EDK shell**	**Sighting #:** 1607124995 **Affected Component:** CM **Impact:** Thunderbolt-SSD connected behind the TBT device are not enumerating in BIOS and EDK shell. **Fix:** Added delay to wait for links to come up before *acking* connect topology command.	**All**

Issue Fixed in Release #	Title	Details	Affected SKUs
71.0	**TBT controller does not get in to RTD3 when one of PCIE controllers are in reset state**	**Sighting #:** 2207495926 **Affected Component:** LC **Impact:** Thunderbolt controller does not get in to RTD3 even when one of the PCIE controllers are disabled/strapped out. **Fix:** Add PERST indication to RTD3 entry condition	**All**
70.0	**Cat-error observed during unplug and plug of Tapex card in S3 state**	**Sighting #:** 1607175843 **Affected Component:** LC **Impact:** Cat-error observed during unplug and plug of the Tapex card in the S3 scenario. **Fix:** LC FW will ignore *ACK* from LSx, if it gets gated with domain reset request.	**All**
70.0	**P2P connection is not enumerating while swapping the ports during S4 cycle with TBT3 Akitio SP storage.**	**Sighting #:** 1607203965 **Affected Component:** CM **Impact:** Sporadically P2P connection is not enumerating while swapping the ports during S4 cycle with TBT3 Akitio SP storage. **Fix:** TBT FW will disconnect the device if the cable_info is cleared during the Link bring up.	**All**
69.0	**Corrupted Vendor/Model names in Device_connected_notification of AR device**	**Sighting #:** 1306400491 **Affected Component:** CM **Impact:** Corrupted Vendor/Model names displayed in Device_connected_notification of AR device. **Fix:** Reads the DWORD aligned buffers from AR device NVM.	**All**
69.0	**Device wake configuration**	**Sighting #: N/A** **Affected Component:** CM **Fix:** Restoring the device wake configuration back to default during SX entry, in case it was different from default.	**All**
69.0	**Merging fixes to default NVM**	**Sighting #: N/A** **Affected Component:** CM/LC **Fix:** Merge latest fixes between binary SKUs.	**All**
68.0	**CATERR observed in S3/S4 cycles on ICL**	**Sighting #:** 1607154750 **Affected Component:** LC **Impact:** On an ICL RVP, CATERR's with post codes b503 and b504 are noticed when the system enters the S3 and S4 cycles respectively.	**All**
68.0	**Change presets value**	**Sighting #:** 1409251995 **Affected Component:** LC **Fix:** TBT FW is updated in order to adjust the TX presets.	**All**

Issue Fixed in Release #	Title	Details	Affected SKUs
67.0	**P2P functionality fails during multiple hot plugs in S0 state**	**Sighting #:** 1607134976 **Affected Component:** DP **Fix:** Fixed in TBT FW wherein we are increasing the CM Buffer to avoid over-run overrun and IOM FW that has a fix for TC Cold for update Cable Info registers.	**All**
67.0	**USB-C to DP display is not enumerating during S3**	**Sighting #:** 1607094600 **Affected Component:** CM **Fix:** Increasing stack size from 0x700 to 0x900.	**All**
66.0	**CATERR on S3/S4 Exit when connected with TR EP + USB3 drive**	**Sighting #:** 1606775814, 1806785026 **Affected Component:** LC/CM **Impact:** CATERR is seen during S3/S4 cycles when connected TR dock or Tapex with USB3 drive. **Fix:** Send *Go2SX* command to CM only after PCIE RP is in D3 state	**All**
66.0	**CATERR on restart with AR dock + DP**	**Sighting #:** 1606682090 **Affected Component:** LC/CM **Impact:** CATERR observed at PC 0000 while performing Restart cycle with Two 4k display connected behind the TBT3 AR dock	**All**
66.0	**Sporadic autowake from S3/S4 fix**	**Sighting #:** 1607081833 **Affected Component:** LC/CM **Impact:** Sporadic autowake is observed from S3/S4 cycles with device populated behind the TBT3/TBT2 docks	**All**
66.0	**Wake using keyboard/mouse connected behind TBT3 dock**	**Sighting #:** 1606951643 **Affected Component:** LC/CM **Impact:** Wake from USB Keyboard/Mouse behind TBT3 docks (AR/TR) is not working from S3/S4 sporadically	**All**
64.0	**Disable CL1**	**Sighting #:** 1306115076 **Affected Component:** CM **Fix:** Disable CL1 (only CL0s is enabled) in order to avoid CIO link hang on training after few hours of traffic	**All**
64.0	**RTD3 flow enhancement**	**Sighting #: N/A** **Affected Component:** CM **Fix:** RTD3 flow enhancements to improve performance by reducing device flash access.	**All**
63.0	**Support for quick restore**	**Sighting #: N/A** **Affected Component:** DP **Impact:** DP OUT would use TPS4 in case LT is performed in HBR3 and max TPS known is TPS2.	**All**

Issue Fixed in Release #	Title	Details	Affected SKUs
63.0	**PHY TX CTS**	**Sighting #: N/A** **Affected Component:** DP **Impact:** Support for test request when AUX request comes in as a burst (reading of 0x201 + some more DPCD registers).	**All**
63.0	**Vendor Specific Register**	**Sighting #: N/A** **Affected Component:** DP **Fix:** Fix for the corner case, where LC might change the DP plug state close to C10 entry.	**All**
63.0	**RTD3**	**Sighting #: N/A** **Affected Component:** DP **Fix:** Changes made to support RTD3.	**All**
62.0	**DP plug state close to C10 entry**	**Sighting #: N/A** **Affected Component:** DP **Fix:** Fix for the corner case, where LC might change the DP plug state close to C10 entry.	**All**
62.0	**RTD3 flow enhancement**	**Sighting #: N/A** **Affected Component:** CM **Impact:** Made some RTD3 flow enhancements to avoid conflict in Thunderbolt.	**All**
62.0	**CATERR on USB device Plug/Unplug**	**Sighting #:** 1306170663 **Affected Component:** LC **Impact:** When the usb device is plugged/unplugged during S0, CATERR is noticed. **Fix:** W/A added to address this issue	**All**
61.0	**Redundant DP plug events**	**Sighting #:** 1408276904 **Affected Component:** CP **Impact:** DP adapter ports on the thunderbolt controller, were sending plug event packets even when no device was connected. **Fix**: Block redundant DP plug events after C10.	**All**
61.0	**P2P connection**	**Sighting #:** 1305999339 **Affected Component:** CM **Impact:** P2P functionality is not working when P2P connection is done during/after Sx cycle. **Fix:** Addressed by addressing CM-Driver interaction.	**All**
61.0	**CATERR on Sx Entry**	**Sighting #:** 1305909590 **Affected Component:** LC **Impact:** System throws CATERR on Sx Entry with TBT Legacy Devices (Port Ridge). **Fix:** Addressed by Sx transition LC handling.	**All**